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# Reliability Evaluation of Glass Interposer Module

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## ABSTRACT

In this paper, we investigate reliability testing for a glass interposer. The test vehicle is an assembled glass interposer with a chip, a BT substrate. The structure of a glass interposer with two redistribution layers (RDLs) on the front-side and one RDL on the back-side has been evaluated and developed. Key technologies, including via fabrication, front-side RDL formation, microbumping, temporary bonding, glass thinning, and back-side RDL formation, have been developed and integrated for high performance. The BT substrate design and PCB for electrical characterization of reliability tests are reported in this paper. The results indicate that this glass interposer can be integrated. The data show the feasibility of this glass interposer for electronics applications.

## INTRODUCTION

Through glass via (TGV) interposer fabrication processes are critical techniques in three-dimensional integrated circuit (3D-IC) integration, providing short interconnections among different stacked chips and substrates. Currently, silicon is a mature material in semiconductor technology, but glass, a dielectric material, provides an attractive option because its intrinsic characteristics offer the advantages of electrical isolation, better RF performance, flexibility with CTE, and most importantly, low cost. Numerous papers have demonstrated Si interposers with 2.5D or 3D stacking integration because Si has a CTE match with Si ICs. Furthermore, silicon infrastructure, including foundry wafer processes and the support for Si equipment, is widely available. A silicon interposer is also an effective solution for high pin-count IC applications based on mature Si technologies such as advance via formation and fine line Cu damascene multilevel interconnection processes. However, silicon interposers have several problems that glass interposers do not have: (1) Si is a semiconductor and not a good conductor or insulator; (2) large CTE differences between Cu and Si obstruct through silicon via (TSV) formation processes; (3) silicon is costly due to the need for electrical insulation around the via sidewall; and (4) the wafer size is limited based on the constraints of the silicon industry. Mass production requires reduced costs; the consensus regarding the cost of ownership is “the cheaper, the better.” Instructive examples of such low aspect ratio applications include CMOS Image Sensors for wafer-level processes [1-4].

A striking challenge of 3DIC engineering is thermal throttling when multi chips are stacked together. The signal performance is limited by a chip to chip thermal coupling effect. It is a challenge to decrease that coupling effect because chip features are small. One promising solution is to use a substrate with low thermal conductivity, such as glass. Because of the very low thermal conductivity of glass, the equivalent thermal conductivities, $k_{xy}$ and $k_z$, of a TGV interposer are both much lower than those of a TSV interposer. Simulation work for the thermal characteristics of a glass interposer has been studied extensively in Ref. [5]. Comparisons of the electrical designs, simulations, and measurement analyses regarding thermal performance have been studied in Ref. [6] and Ref. [7]. This paper considers glass interposer characterization, wafer-level integration, assembly, and fabrication, and also electrical and thermal properties.

## I. EXPERIMENTAL

*Glass interposer*

An interposer includes a substrate and two metal layers disposed on the opposite sides of the glass substrate. The interposer (100 μm) is fabricated on a 12” glass substrate. The original thickness for glass substrate is 700 μm and the TGVs are formed directly on a glass wafer by Corning Incorporated. After TGV filling and Cu overburden removed, the top RDL (line-width/space = 3 μm/3 μm), a Cu plating process with a seed layer (Ti/Cu) wet-etching process is applied. A polymer-lithographic material is used for passivation, the highest temperature of the curing process is 200˚C. Top UBM (22 μm in diameter; 6-μm-thick Cu with electroless PdAu) is formed with a top passivation opening (12 μm). Wafer thinning starts with a temporary bonding with a carrier at the front-side (glue thickness = 60 μm). Grinding/CMP is used to reveal the Cu. The bottom RDL is then formed by Cu plating after lithography patterning. The bottom UBM (85–120 μm in diameter) is formed with a polymer passivation opening of 85–120 μm.

*Assembled with chip, BT substrate and PCB.*

The BT substrate design and PCB for electrical characterization of reliability test is included in this work. The reliability test vehicle is shown in Figure 1. We checked the electrical properties of the assembly module step by step; then, we finished the assembly of the chip with a glass interposer, a BT substrate and a PCB.


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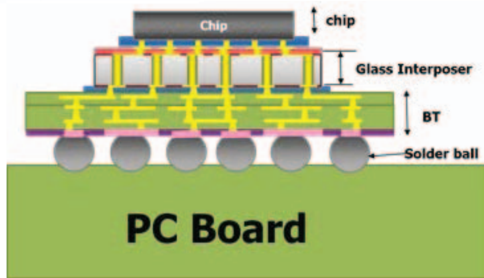


**Figure 1 Assembly module for test vehicle**

III. RESULT AND DISCUSSION

The glass interposer is composed of 100-µm-thick glass with two RDLs on the front-side and one RDL on the back-side. The major differences between the glass process and the Si interposer process are the methods of via formation and isolation. Glass material is composed with $SiO_x$, which provides insulation for electrical currents. A polymer-based dielectric layer is used for insulation and passivation; the equipment and process for polymer-based dielectric layer isolation are more cost-effective than oxide or nitride inorganic-based isolation. The vias of the glass interposer are formed by Corning Incorporated via drilling technology. The via size is reduced to 25 µm from 30 µm. A real glass interposer with two RDLs on the front-side and one RDL on the back side is shown in Figure 2.

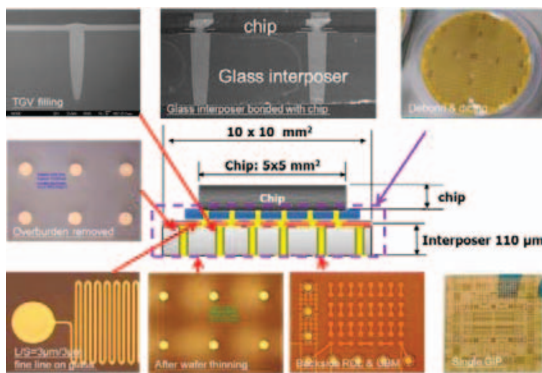


**Figure 2 structure for glass interposer**

*Assembly of Chip-to-Glass interposer on Organic Substrate*

The chip was stacked on the BT substrate by a two-step assembly process. The first step was the joining of the glass interposer and substrate by a reflow process. Assembly of the glass interposer on the substrate was conducted in a five-zone reflow oven. The glass interposer with flux dipping was properly aligned onto the substrate and subsequently reflowed for soldering. The reflow profile had a peak temperature of 245°C and a dwell time of 60 seconds above liquids; this ensured that the soldering between glass interposer and substrate would meet quality criteria.

Once the glass interposer module was completed on the BT substrate, the second step consisted of microbump soldering between chip and glass interposer by a flux-enhanced thermocompression bonding process. The usage of flux was very important in this stage. Because solder bumps and microbumps had been fabricated onto the back-side and front-side of the glass interposer respectively, the microbumps were reflowed for a short time and an oxidation layer formed on those microbumps. Therefore, to construct interconnections between the chip and glass interposer, thermocompression bonding with flux was required. Cross-sectional analysis of the microstructures of the chip-stack substrate module was conducted to determine bonding conditions. Bonding conditions of 250°C/10 sec under gap-height control mode were used.

Figure 3 shows the real assembled substrate module and an X-ray image of its solder-bump joints and microbump joints, which have different pitch values. Figure 3 shows that the edge solder-bump joints and microbump joints were correctly aligned, which was necessary for the success of this two-step chip-stack substrate module assembly process.

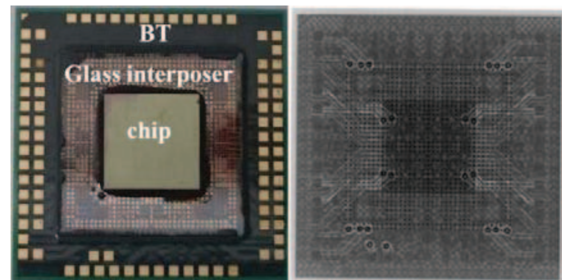


**Figure 3 Assembled substrate module and its X-ray image**

Figure 4 shows cross-sectional images of the chip-stack, the BT substrate, and the microstructures of the solder joints. This image shows that the microbump interconnections were joined securely even though voids existed within the microjoints. As can be seen from this image, 100-µm-pitch and 150-µm-pitch interconnects were aligned and joined properly. These photographs confirmed that flux-enhanced thermocompression bonding produced high-quality microbump joining. The contact resistance levels of the microjoints were measured on the glass interposer module. Figure 5 shows a plot of contact resistance distributions obtained by measuring various sets of microjoints. Spots with 150 µm bump pitch on the glass interposer were connected with 26 I/O bumps, TGV, 2 RDL on the front-side and 1 RDL on the back-side. The measured contact resistance of the microjoints included the resistance of the metal traces. Figure 5 shows measurements of contact resistance levels between chip, glass interposer, and BT substrate. The resistance of a daisy chain for 150 µm bump pitch with TGV was approximately 15Ω.

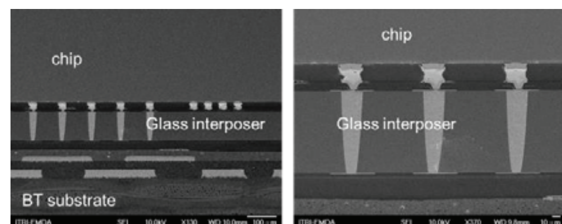



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**Figure 4. Cross-sectional views of microstructures of microbump joints and TGVs**

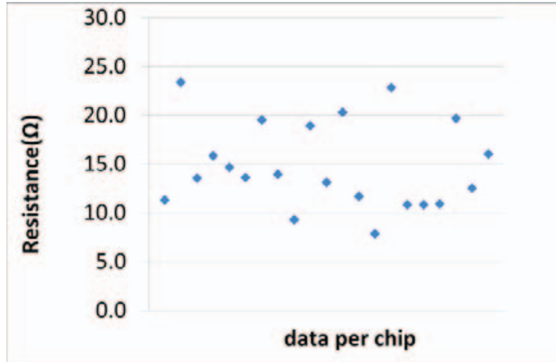


**Figure 5 Plot of contact resistance distribution was obtained by measuring various chips of microjoints. One spot was the average contact resistance per chip, every chain within chip on the glass interposer is 150 μm bump pitch that was connected with 26 I/O bumps, TGV, 2 RDL on the front-side, and 1 RDL on the back-side;**

*Reliability test*

The reliability levels of the glass interposer and that of the glass interposer with chip, and BT assembled by thermocompression bonding (TCB) were assessed by TCT (TCT, Thermal Cycling Test). The TCT conditions for each cycle were –55ºC – 125ºC; Dwell time = 5 min; Ramp rate = 15ºC / min. After 500 cycles of TCT, the electrical property is similar to original (Fig. 6).

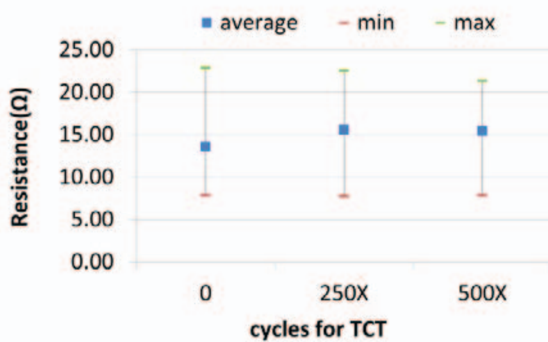


**Figure 6 Plot of contact resistance distribution was obtained by measuring various chips of microjoints. One spot was the average contact resistance per chip.**

The other reliability test item is high temperature storage (HTS), the structure of samples for this test is same to TCT test, and baked at 150ºC, 1000hr. The initial resistance before HTS test is about 15Ω, the resistance during HTS test is within 25Ω. By increasing baking time, the resistance is decreasing.

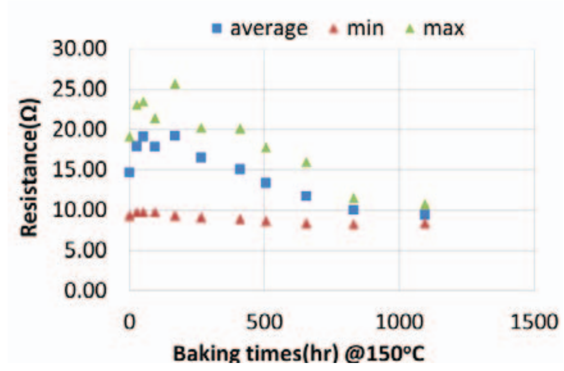


**Figure 7 Plot of contact resistance distribution was obtained by measuring various chips of microjoints. One spot was the average contact resistance during baking.**

For drop test, we follow the JEDEC standard to design PCB and assemble the BT module on it (Fig. 8). The assembly process is on-going.

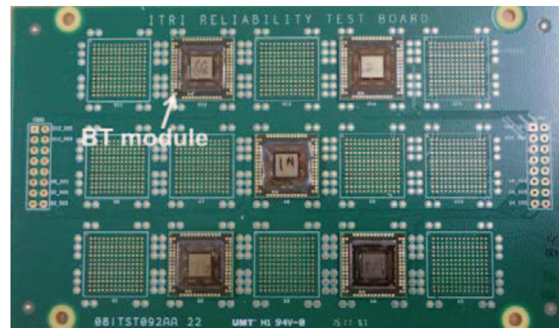


**Figure 8 PCB module for drop test.**

## IV. CONCLUSION

A wafer-level 300mm glass interposer scheme with top-side RDL, Cu TGVs, back-side RDL, Cu/Sn microbumps, and polymer passivation has been implemented. A device has been assembled with a chip, a BT substrate and PCB. For reliability, the samples were past to the 500cycles for TCT tes and 1000hrs for HTS test. The drop test is ongoing.

1. In this investigation, an optimized process was applied for the glass interposer. A polymer-based dielectric material was used for passivation. The top diameter of TGV was 25 μm. A top UBM (22 μm in diameter; 6-μm-thick Cu with electroless PdAu) was formed with a top passivation opening (12 μm).

2. For a reliability test vehicle, the glass interposer was assembled with a chip, a BT substrate. The bonding process was optimized and properly connected solder microbump joints can be formed between chip, glass interposer, and BT substrate. The average resistance of a daisy chain for 150 μm bump pitch with TGV was about 15Ω.


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3. After 500 cycles of TCT, the electrical property is about 15 15Ω and similar to original.

4. For high temperature storage(HTS), the initial resistance before HTS test is about 15Ω, the resistance during HTS test is within 25Ω.

## ACKNOWLEDGMENT

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